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09/654,527	09/01/2000	Hideo Miyake	1614.1074	7021

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EXAMINER	
MEONSKE, TONIA L	
ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 09/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/654,527	MIYAKE ET AL.	
	Examiner	Art Unit	
	Tonia L. Meonske	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8,11-13,15 and 16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,11-13,15 and 16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/28/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-8, 11-13, 15, and 16 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Faraboschi et al., US Patent 5,930,508 (herein referred to as Faraboschi).

3. Referring to claim 1, Faraboschi has taught a parallel processor performing parallel processing of one or more basic instructions contained in each of a plurality of instruction words delimited by instruction delimiting information, said parallel processor comprising:

a. a plurality of instruction execution units performing processes in accordance with corresponding, supplied basic instructions in parallel (Abstract, Figures 1, 7, and 9, Functional units,);

b. an instruction fetch unit fetching the instruction words one by one in accordance with the instruction delimiting information to generate a first instruction word format (column 5, line 45-column 6, line 19, Figure 6, element 630 is a first instruction word format stored in the alignment buffer, element 730 of Figure 7.); and

c. an instruction issue unit recognizing and, in accordance therewith, selectively issuing each of the basic instructions supplied from the instruction fetch unit to one of the

corresponding instruction execution units to execute the issued basic instruction (Abstract, Figures 1, 6, 7, and 9, column 4, line 57-column 5, line 4);

d. wherein the instruction issue unit comprises a conversion unit (Figure 6, element 640) to generate an interface having effective bits (column 4, lines 56-66, D bits are interfaced to the conversion unit.) and a second instruction word format (Figure 6, element 650 stored in element 750 or Figure 7) based on a type of instruction words and the first instruction word format (Instructions are converted based on type because the opcode, or type of instruction, is converted to the new instruction format, element 650, based on the first instruction word format, element 630.), the effective bits indicating availability of the corresponding instruction execution units (Merriam-websters online dictionary defines "available" as "qualified or willing to do something or to assume a responsibility." The effective bits indicate the availability of the corresponding execution units by indicating which functional unit assumes the responsibility of executing the instruction.) and the second instruction word format indicating a second arrangement of the basic instructions corresponding to an arrangement of the instruction execution units (Figure 6, The second arrangement is in element 650, such that NOP are inserted into the arrangement.).

4. Referring to claim 2, Faraboschi has taught the parallel processor as claimed in claim 1, as described above, and wherein the plurality of instruction execution units all have the same structure (column 4, lines 46-48, All of the instruction units have arithmetic units.).

5. Referring to claim 3, Faraboschi has taught the parallel processor as claimed in claim 1, as described above, and wherein:

a. at least two of the instruction execution units have different structures from each other (column 4, lines 46-48, Arithmetic units and multipliers are different structures.); and

b. the instruction fetch unit rearranges the basic instructions contained in each of the fetched instruction words, in accordance with arrangement of the plurality of instruction execution units, and then supplies the rearranged basic instructions to the instruction issue unit (Abstract, Figures 1, 6, 7, and 9, column 4, line 57-column 5, line 4, column 5, line 45-column 6, line 19, elements 720, 730, 740, and 750).

6. Referring to claim 4, Faraboschi has taught the parallel processor as claimed in claim 1, as described above, and wherein:

a. at least two of the instruction execution units have different structures from each other (column 4, lines 46-48, Arithmetic units and multipliers are different structures.); and

b. the instruction issue unit rearranges the basic instructions contained in each of the instruction words supplied from the instruction fetch unit, in accordance with arrangement of the plurality of instruction execution units, and then supplies the rearranged basic instructions to the instruction execution units (Abstract, Figures 1, 6, 7, and 9, column 4, line 57-column 5, line 4, column 5, line 45-column 6, line 19, elements 720, 730, 740, and 750).

7. Referring to claim 5, Faraboschi has taught the parallel processor as claimed in claim 1, as described above, and wherein:

a. at least two of the instruction execution units have different structures from each other (column 4, lines 46-48, Arithmetic units and multipliers are different structures);

b. the instruction fetch unit rearranges the basic instructions contained in each of the fetched instruction words, in accordance with arrangement of the instruction execution units (column 5, line 45-column 6, line 19, Figure 6, element 630 is a first instruction word format stored in the alignment buffer, element 730 of Figure 7. This stored instruction word is in accordance with the arrangement of execution units.), and

c. then supplies the rearranged basic instructions to the instruction issue unit (Figure 7); and

d. the instruction issue unit further rearranges the basic instructions contained in each of the instruction word supplied from the instruction fetch unit, in accordance with the arrangement of the instruction execution units, and then supplies the rearranged basic instructions to the instruction execution units (Abstract, Figures 1, 6, 7, and 9, column 4, line 57-column 5, line 4, elements 640, 740, and 750.).

8. Referring to claim 6, Faraboschi has taught the parallel processor as claimed in claim 3, as described above, and wherein:

a. at least two of the instruction execution units have different structures from each other (column 4, lines 46-48, Arithmetic units and multipliers are different structures.); and

b. the instruction fetch unit fetches an instruction word that contains basic instruction arranged in advance in accordance with the arrangement of the instruction execution units (column 5, line 45-column 6, line 19, Figure 6, element 630 is a first

instruction word format stored in the alignment buffer, element 730 of Figure 7, in advance of execution.).

9. Referring to claim 7, Faraboschi has taught the parallel processor as claimed in claim 1, as described above, and wherein, depending on the type of a basic instruction being currently executed by one of the instruction execution units, the instruction issue unit issues a next basic instruction before the execution of the basic instruction being currently executed is completed (column 4, lines 46-50).

10. Referring to claim 8, Faraboschi has taught the parallel processor as claimed in claim 7, as described above, and wherein, if a supplied basic instruction does not have data dependency or control dependency, or does not share resources with a basic instruction being currently executed by one of the instruction execution units, the instruction issue unit issues the supplied basic instruction before the execution of the basic instruction being currently executed is completed (column 4, lines 46-50, column 1, lines 16-62).

11. Referring to claim 11, Faraboschi has taught a parallel processor as claimed in claim 1, as described above, and wherein a

a. first instruction word format is converted into a second instruction word format, the first instruction word format indicating a first arrangement of instruction words from the instruction fetch unit (Figures 6 and 7, elements 620, 630, 720, and 730), and the second instruction word format indicating a second arrangement of instruction words which corresponds to the instruction execution units (Figures 6 and 7, elements 640, 650, 740, and 750).

12. Referring to claim 12, Faraboschi has taught a parallel processor as claimed in claim 1, as described above, and wherein the conversion unit converts a first instruction word format into a second instruction word format on the basis of the effective bit, corresponding to the instruction execution units, indicating whether the corresponding instruction execution unit is available (Figures 6 and 7, The effective bits indicate the availability of the corresponding execution units by indicating which functional unit assumes the responsibility of executing the instruction. The conversion performed by element 740 uses the effective bits to expand the instruction in element 650 such that NOP's are inserted into the new instruction format.).

13. Referring to claim 13, Faraboschi has taught a parallel processor as claimed in claim 12, as described above, and wherein the first instruction word format indicates a first arrangement of instruction words from the instruction fetch unit (Figures 6 and 6, elements 620, 630, 720, and 730), and the second instruction word format indicates a second arrangement of instruction words which corresponds to the instruction execution units (Figures 6 and 6, elements 640, 650, 740, and 750).

14. Referring to claim 15, Faraboschi has taught a parallel processor as claimed in claim 1, as described above, and wherein the instruction issue unit issues the basic instructions to the corresponding instruction execution unit based on the interface (Figures 6 and 7, The expansion logic issues the instructions to the disbursed instruction buffer.).

15. Referring to claim 16, Faraboschi has taught a parallel processor performing parallel processing of one or more basic instructions contained in each of a plurality of instruction words delimited by instruction delimiting information (Figures 5 and 6), said parallel processor comprising:

a. a plurality of instruction execution units performing processes in accordance with corresponding, supplied basic instructions in parallel (column 4, lines 46-50, column 1, lines 16-62, Figure 1);

b. an instruction fetch unit fetching the instruction words one by one in accordance with the instruction delimiting information to generate a first instruction word format (column 5, line 45-column 6, line 19, Figure 6, element 630 is a first instruction word format stored in the alignment buffer, element 730 of Figure 7.);

c. an interface having effective bits corresponding to the instruction execution units (column 4, lines 56-66, D bits) and a second instruction word format based on a type of instruction words and the first instruction word format (Figure 6, element 650 stored in element 750 or Figure 7), the effective bits indicating the corresponding instruction execution unit for each instruction word (column 4, lines 56-66, D bits);

d. wherein the instruction words fetched by the instruction fetch unit have no attached dispersal information (Figure 6, element 630 stored in element 730 does not have the NOP dispersal information attached to element 650 stored in element 750.), and the effective bits are based on and the second instruction word format indicating a second arrangement of the basic instructions corresponding to an arrangement of the instruction execution units (The effective bits represent the arrangement of the second instruction word format, which corresponds to the arrangement of the execution of instructions in the functional units.).

Response to Arguments

16. Applicant's arguments with respect to claims 1-8, 11-13, 15, and 16 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L. Meonske whose telephone number is (571) 272-4170. The examiner can normally be reached on Monday-Friday, with every other Friday off.

18. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie P. Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

19. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

tlm

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